IN THE CLAIMS

1. (Previously Presented) A method for stacked register aliasing in data hazard detection of a processor, comprising the steps of:

identifying a first group of registers within a register file of the processor;

aliasing the first group of registers to first register identifiers;

detecting data hazards, if any, associated with the first register identifiers;

identifying a second group of registers within the register file;

aliasing the second group of registers to second register identifiers; and

detecting data hazards, if any, associated with the second register identifiers, wherein the first and second register identifiers overlap in hazard detect logic across two or more rows of the register file.

2. (Previously Presented) The method of claim 1, each of the steps of identifying comprising identifying registers within a 128-register register file.

3. (Previously Presented) The method of claim 2, the steps of detecting comprising utilizing groups of 32 register identifiers to alias data hazard detect logic to windows of 32-register frames.

4. (Currently Amended) A processor for processing program instructions, comprising:

a register file grouped into two or more non-overlapping equally sized stacks of consecutive registers;

an execution unit having an array of pipelines for processing the instructions and for writing bypass data to the register file; and

data hazard detect logic for detecting ~~and aliasing data hazard detection for two or more rows of the register file~~ data hazards in the bypass data without differentiation between corresponding registers of each stack.

5. (Currently Amended) The processor of claim 4, further comprising a register ID file for facilitating data hazard detection ~~associated with rows of the register file~~, the register ID file having a plurality of register identifiers, the data

hazard detect logic aliasing data hazard detection according to mapping of the register identifiers to corresponding registers of each stack.

6. (Previously Presented) The processor of claim 5, the register ID file mapping sequential 32-registers with the common hazard logic to more than 32 stacked registers of the register file to alias in 32-register sequences.

7. (Currently Amended) In data hazard detect logic of a processor of the type having a register file and a register ID file providing row-to-row data hazard detection, the improvement wherein each register ID of the register ID file ~~ID~~ aliases row-to-row hazard detection of the register file by common data hazard detection logic for two or more non-consecutive rows of the register file.

8. (Currently Amended) A method for data hazard detection within a processor, comprising:

aliasing each register identifier of a group of register identifiers to two or more registers of a register file of the processor, the register file formed of equally sized non-overlapping groups of consecutive registers, each of the register identifiers aliasing one corresponding register of each group of registers; and

determining data hazards within the register file by ~~processing~~ comparing one or more of the register identifiers.

9-10. (Cancelled)

11. (Previously Presented) The method of claim 8, wherein the step of aliasing increases the register file size without a corresponding increase in data hazard detection logic.

12. (Previously Presented) The method of claim 8, wherein the group of register identifiers has 32 register identifiers.

13. (Currently Amended) A method of reducing data hazard logic dependency on size of a register file within a processor, comprising:

selecting a register ID file size;

aliasing at least one entry of the register ID file to two or more registers of the register file, each of the two or more registers being located in a non-overlapping group of sequential registers equivalent in size to the selected register ID file size; and

evaluating matches between entries of the register ID file in the hazard logic without distinguishing between common aliased entries of the register file.

14. (Previously Presented) The method of claim 13, wherein the step of aliasing increases the register file size without a corresponding increase in data hazard detection logic.

15. (Currently Amended) A method of data hazard detection within a processor, comprising:

aliasing each register ID within data hazard detection logic to two or more non-consecutive registers of a register file; and

determining data hazards by matching register IDs within the data hazard logic.

16. (Currently Amended) A method for stacked register aliasing in data hazard detection logic of a processor, comprising:

aliasing two or more non-overlapping groups of consecutive registers of a stacked register file to one group of consecutive register IDs within the data hazard detection logic, each register ID aliasing one register from each group of consecutive registers; and

detecting data hazards, if any, associated with a first and second register of the ~~two or more groups~~ stacked register file by comparing a first aliased register ID of the first register to a second aliased register ID of the second register within the data hazard detection logic.;

~~wherein each register ID aliases to one register of each of the two or more groups of registers, the two or more groups of registers overlapping in hazard detect logic~~.

17. (New) The method of claim 12, wherein each group of consecutive registers has 32 registers.